

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	83625	(circuit transistor) near8 (layout arrengment matrix)	US-PGPU B; USPAT; USOCR	OR	ON	2007/02/27 16:00
L2	492	1 and (four near5 four near5 (Layout arrengment matrix))	US-PGPU B; USPAT; USOCR	OR	ON	2007/02/27 16:00
L3	65990	(circuit transistor) and (layout arrengment matrix)	FPRS; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2007/02/27 16:00
L4	1348	3 and (four same four same (Layout arrengment matrix))	FPRS; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2007/02/27 16:01
L5	55	3 and (four near8 four near8 (Layout arrengment matrix))	FPRS; EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2007/02/27 16:48